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PATENT ABSTRACTS OF JAPAN

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MACHIDA TETSUSHI
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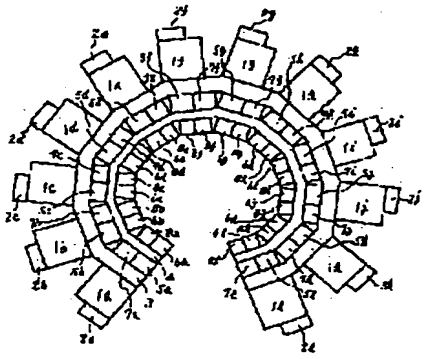
(54) FORMATION METHOD OF RESIST PATTERN

(57)Abstract:
PURPOSE: To prevent a drop in the efficiency of a treatment and to enhance the productivity of the title method by a method wherein a resist coating treatment, an exposure treatment and a development treatment are formed of groups composed of parallel and independent treatment parts and the connection between treatment groups is provided with a degree of freedom.
CONSTITUTION: An interface unit 3 is provided with an interface function and a conveyance function which can freely deliver a wafer to exposure-device main bodies 1a to 1l. Photoresist-coating treatment units 5a to 5l and development treatment units 7a to 7l. are arranged at its inside. The wafer can be delivered freely between the units and the unit 3. A conveyance unit 4 is arranged at the inside of the treatment units 5a to 5l and the units 7a to 7l. The conveyance unit 4 delivers the wafer among baking treatment units 6a to 6l, 8a to 8l, the treatment units 5a to 5l and the development treatment units 7a to 7l. Thereby, it is possible to eliminate that the waiting time for a wafer treatment is caused due to the difference in the treatment capacity of the treatment units.



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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the formation method of the resist pattern in a phot lithography processes of semiconductor fabrication machines and equipment.
[0002]
[Description of the Prior Art] A phot lithography technology is the foundations of the micro-processing process of LSI, and the success or failure of micro processing of LSI are dependent on the precision of this process. A phot lithography processes are also called pattern imprint process, start in a photoresist application, and are completed by etching of a pattern, and removal of a photoresist through pattern exposure and development. Technically, these have an indivisible relation, and in order that it it may pull out the performance of other processes, they have a relation of being devised and used.
[0003] The relation of the formation method of the resist pattern of a phot lithography processes and the resist coater in this process, an aligner, and a developer is explained using drawing 15 . This drawing shows the process of a typical resist pattern, and shows the process with the flow chart in order. First, the 1st BEKU (DEHAIDOROESHOMBEKU) is given to the 1st at a wafer-like semiconductor substrate (henceforth a wafer), and the moisture of the minute amount which remains on a wafer front face is removed. Although the throughput of this process is based also on the setups, generally a 6 inches wafer is about 40-80 sheets at unit time (for example, 1 hour).
[0004] Processing of photoresist coating is performed after the 1st BEKU. In this photoresist coating, a uniform thin film is formed for the photoresist which makes an organic material a principal component on a wafer front face for example, by the spin coat method. Generally the throughput of this photoresist coating is about 40-80 sheets with a 6 inches wafer at unit time (for example, 1 hour).
[0005] Next, the 2nd BEKU (pulley exposure BEKU) is given. In this process, the photoresist solvent (usually organic solvent) which remains in the photoresist film formed on the wafer front face is removed. Generally, the process of the 1st above-mentioned BEKU, photoresist coating, and the 2nd BEKU is continuously processed using a resist coater.
[0006] Next, exposure processing is performed to a photoresist film and the resist pattern corresponding to the circuit pattern is formed. As an aligner used for exposure processing, there are the following, for example. As a thing using ultraviolet rays and far ultraviolet rays as a light used for exposure, there are a reduction projection aligner (stepper), a reflective projection aligner, a reflective reduction projection aligner, etc., and there is an EB exposure machine (electron-beam-exposure machine) as a thing using an electron ray, in addition the thing using an X-ray or an ion beam is known. Generally the 6 inches wafer of the throughput at the time of using a stepper is about 20-80 sheets at unit time.
[0007] The 3rd BEKU (post exposure BEKU) is given to the wafer exposed by the aligner, and generating of the phenomenon generally called standing wave is suppressed. Generally the 6 inches wafer of the throughput of this processing is about 40-80 sheets at unit time. A development is given after this 3rd BEKU and a resist pattern is formed. Generally the 6 inches wafer of the throughput of this processing is about 20-60 sheets at unit time. A direct development may be performed without performing processing of the 3rd BEKU if needed and performing

processing of this 3rd BEKU after exposure processing.
[0008] As for a wafer, the 4th BEKU (POSUTODEBEROPPUBEPU) is given after a development. The rinse (used for washing of the developer after a development) of the minute amount which remains on the front face of the resist pattern after a development, the interior, and a wafer front face is removed by this processing. Generally the 6 inches wafer of the throughput of this processing is about 40-80 sheets at unit time. Generally, the 3rd BEKU, development, and processing of the 4th BEKU are continuously processed in a developer.
[0009] Then, it is sent to the following process through inspection of a resist pattern. In drawing 3 , the conventional arrangement of the equipment by which the above-mentioned process is processed is explained. What is shown in drawing is the example of the automatic delivery method called in-line method, and 12 lines are shown. Each line is the same composition and each has the composition of having become independent. Line a explains a processing line.
[0010] BEKU processing unit 26a to which, as for Line a, the 1st BEKU and the 2nd BEKU are performed, The resist coater which consists of photoresist coating processing unit 25a to which photoresist coating is performed, The developer which consists of the aligner to which exposure processing is performed, BEKU processing unit 28a to which the 3rd BEKU and the 4th BEKU are performed, and development unit 27a to which development is performed, Conveyance unit 24a which conveys a wafer between the BEKU processing units 26a and 28a, photoresist coating processing unit 25a, and development unit 27a, It consists of in-line face unit 23a which conveys a wafer between an aligner main part, a resist coater, and a developer.
[0011] The aligner consists of aligner main part 21a and rack 22a. Other Lines b - Lines l are the same composition as Line a, and same processing is performed. Line a - Line l are the composition of having become independent, respectively, and processing of the line here is performed, without being influenced by processing of other lines. The number of work concerning [automatic and continuous wafer processing is possible for the formation method of the resist pattern described above, and] a help can be decreased. Adhesion to the wafer of the dust which this produces from the human body which is one of the poor causes of LSI can be decreased remarkably. Therefore, the ratio of the operating time of equipment can be raised. This can do a great effect so in a mass-production process.
[0012]
[Problem(s) to be Solved by the Invention] However, there were the following troubles by the above-mentioned method.
(1) When the throughputs of the processor in each process differ, respectively, that is, the processing number of sheets of the wafer around unit time differs, the processor-limited time of a wafer will arise. If the number of processing units of down stream processing with little processing number of sheets is made the same like BEKU processing or photoresist coating processing like the number of processing units of down stream processing with much processing number of sheets, and an aligner and a developer, when progressing to down stream processing with little processing number of sheets from down stream processing with much processing number of sheets, it is necessary to stand by until the last processing in the following process ends a wafer. Moreover, if the installation number of an aligner or a development unit is increased too much, in case it will progress to the following processing unit from an aligner or a development unit conversely, the time of a wafer processor limited will arise.
[0013] (2) Moreover, it has set on the processing line, and may shift and the situation which processing of the processing unit stops fixed time may arise by failure or the periodical maintenance service in that processing unit. Under the present circumstances, the processing line in which this stopped processing unit is contained must suspend all processings, and will also stop a normal processing unit.
[0014] (3) It is possible to remove the processing unit from in-line, and to give the assistance by the help by halt of a processing unit, and the efficiency of processing falls at this time, and further, the dust generated from a human body adheres to a wafer front face, becomes the defect of a circuit pattern, and also affects the incidence of the excellent article of LSI. this invention loses generating of the time of the wafer processor limited produced according to the difference of the

throughput of a processing unit, and prevents a halt of the whole processing line by halt of some processing units, prevents decline in the efficiency of processing and, thereby, aims at providing the formation method of the resist pattern which raises productivity by removing the trouble described above and giving relevance to a processing unit between processing lines.

[0015]

[Means for Solving the Problem] this invention treats the processing unit which performs the same processing in two or more processing line in order to attain the above-mentioned purpose as a unit group of one group which is not as a unit which each became independent of, and was related, and processes by relating the adjoining processing unit group and connecting. This processing unit group is related, and it connects, it relates with each throughput of a processing unit based on the connection, and the number of the processing unit in a processing unit group is defined.

[0016]

[Function] According to this invention, in the formation method of the resist pattern in a phot lithography processes of semiconductor fabrication machines and equipment, two or more down stream processing which performs same processing in two or more processing lines is treated as a processing unit group, those processing units are overlapped and connection between processing unit groups is made.

[0017] A halt of the whole processing line can be prevented by being able to give relevance between processing units, becoming possible to set up the number according to the throughput of each processing unit, and losing generating of the time of the wafer processor limited produced according to the difference of the throughput of a processing unit by this method, and making other processing units distribute processing in the case of a halt of some processing units. Thereby, decline in the efficiency of a phot lithography processes of semiconductor fabrication machines and equipment can be prevented, and productivity can be raised.

[0018]

[Example] Hereafter, it explains in detail, referring to drawing about the example of this invention. Drawing 2 is drawing showing the connection method of the equipment in which the example of this invention is shown, and drawing 4 is drawing showing the connection method of conventional equipment. First, the connection method of the conventional equipment shown in drawing 4 is explained.

[0019] Each processing is classified and explained to three processes of a resist coater, an aligner, and a developer in formation of the resist pattern of a phot lithography processes of semiconductor fabrication machines and equipment. As shown in drawing 4 (a), processing of a resist pattern is performed by two or more lines of lines 1, 2, and 3 in parallel. Each processing line is installed independently, respectively and there is no relation between lines. A line 1 connects the resist coater 1, an aligner 1, and a developer 1 with in-line, respectively, and it comes to constitute it. Also in lines 2 and 3, it is the same. With composition as shown in drawing 4 (a), since the throughputs of the resist coater 1, an aligner 1, and a developer 1 differ, respectively, in case it moves to the following process, there is a possibility that the time of a wafer processor limited may occur.

[0020] Moreover, if failure arises in a part of down stream processing in a processing line as shown in drawing 4 (b), all the lines will stop. In a line 1, it is the case where the developer 1 has stopped and is the case where the resist coater 2 has stopped, in a line 2. When it lapses into a state like drawing 4 (b), as shown in drawing 4 (c), in a line 1, in-line [between an aligner 1 and a developer 1] is canceled, processing by the help is performed, in-line [between the resist coater 1 and an aligner 1 and between an aligner 1 and a developer 1] is canceled in a line 2, and processing by the help is performed.

[0021] The processing by this help will cause elevation of the incidence of decline in processing efficiency, and the defective of LSI. On the other hand, the concept of the method of this invention is explained in drawing 2 . The example of three lines explains like drawing 4 . In drawing 2 (a), similarly, not only the aligner 1 but an aligner 2 and an aligner 3 overlap, and it connects, and not only the aligner 2 but an aligner 1 and an aligner 3 overlap, the resist coater 2 is connected, further, not only the aligner 3 but an aligner 1 and an aligner 2 overlap, and the resist coater 1 is connected

for the resist coater 3. Therefore, the consisting [of the resist coater 1, a resist coater 2, and a resist coater 3] resist coater group is connected with the aligner group which consists of an aligner 1, an aligner 2, and an aligner 3. the aligner group which consists of an aligner 1, an aligner 2, and an aligner 3 between an aligner and a developer similarly, a developer 1, a developer 2, and a developer 3 -- a shell -- the developer group is connected By overlapping and connecting per group, as mentioned above, relevance arises between each processing unit.

[0022] It becomes possible to set up the number according to the throughput of each processing unit, and by giving relevance between each of this processing unit explains below the example which can lose generating of the time of the wafer processor limited produced according to the difference of the throughput of a processing unit. Here, if x, y, and an operating ratio are set [the throughput of the processing units 1 and 2] to alpha and beta for a, b, and the number, the number of processing of the processing units 1 and 2 will be set to axalpha and bybeta, respectively. Since the difference of the throughput of a processing unit is lost and generating of the time of a wafer processor limited is lost by making equal the number of processing of the processing units 1 and 2, what is necessary will be just to set up the number x of a processing unit, and y so that the following formula may be realized.

[0023] An example when a processing unit stops is explained in ax alpha=by beta drawing 2 (b). In a line 1, if the wafer processed by aligners 1 and 3 when the developer 1 stopped is processed by a developer 2 and the developer 3 and an aligner 2 stops, the wafer processed by the resist coater 1, the resist coater 2, and the resist coater 3 will be processed by an aligner 1 and the aligner 3. Therefore, the whole line in which the processing unit stopped like the conventional example shown in drawing 4 is contained does not stop.

[0024] One example of control of processing is explained below. What is necessary is to set [the throughput of the processing units 1 and 2] x, y, and an operating ratio to alpha and beta for a, b, and the number like ****, and considering the case where the number of the processing unit 2 decreases to y', just to control alpha and beta for an operating ratio to fill ax alpha=by'beta.

[0025] Comparison with the Prior art in the number of processing and the thing of this invention is explained below. Have lines 1, 2, and 3 and each consists of processing units 1, 2, and 3. each throughput -- a1, b1, c1, a2, and b -- 2, c2, a3, b3, c3, and an operating ratio -- alpha 1, beta 1, gamma 1, alpha 2, beta 2, gamma 2, alpha 3, beta 3, and gamma 3 **, if it carries out Since according to the Prior art the number of processing accepts it line 3 with a line 2 and drives, when the processing unit 1 of a line 1 stops a2 alpha2+a3 alpha 3 (=b2 beta2+b3 beta3 =c2 gamma2+c3 gamma3)

According to [come out, are and] the thing of this invention a2 alpha2'+a3 alpha3 ' (=b1 beta1+b2 beta2+b3 beta3 =c1 gamma1+c2 gamma2+c3 gamma3)

It becomes.

[0026] Therefore, the whole number of processing is securable by raising operating ratio alpha2 ' and alpha3 '. when the whole number of processing is not securable by raising operating ratio alpha2 ' and alpha3 ', in order [moreover,] to equalize the number of processing between processing units and not to generate the latency time of processing -- an operating ratio beta 1, beta 2, beta 3, gamma 1, gamma 2, and gamma 3 It can change.

[0027] The 1st example of this invention is explained in drawing 1 . In this example, it has considered as the number and the same number of each unit of drawing 3 . [of the conventional example] 12 sets of 12 sets of the aligner main parts 1a-1l. and the control racks 2a-2l. are arranged annularly, and the interface unit 3 is arranged annularly too at the inside. This interface unit 3 is equipped with 12 sets of the aligner main parts 1a-1l., the interface function which can perform delivery of a wafer freely, and the conveyance function.

[0028] Furthermore, inside this interface unit 3, the photoresist coating processing units 5a-5l. and the development units 7a-7l. are arranged, and delivery of a wafer is made freely between the interface units 3. The conveyance unit 4 is arranged at the these photoresist coating processing units 5a-5l. and development units [7a-7l.] inside.

[0029] This conveyance unit 4 delivers a wafer between the BEKU processing units 6a-6l., 8a-8l. and the aforementioned photoresist coating processing units 5a-5l. which have been arranged

further inside, and the development units 7a-7l. Therefore, by the above-mentioned composition, photoresist coating processing units [5a-5l.] either can also receive a wafer by inline processing, and, as for an aligner 1, can deliver a wafer by inline processing by the interface unit 3 with the interface unit 3 from which photoresist coating processing units 5a-5l. Moreover, delivery of the wafer between the arbitrary units between the BEKU processing units 6a-6l., 8a-8l., and the aforementioned photoresist coating processing units 5a-5l. and the development units 7a-7l. is also attained by the conveyance unit 4.

[0030] The 2nd example of this invention is explained in drawing 5 . In the 2nd example of this invention, the BEKU processing units 6a-6l., the photoresist coating processing units 5a-5l. and the BEKU processing units 8a-8l., and the development units 7a-7l. are arranged at aligner main parts [1a-1l.] both sides. Moreover, in this example, the BEKU processing units 6a-6l. and the photoresist coating processing units 5a-5l. are arranged in the center, and it has become the both sides with the composition that the aligner main parts 1a-1f, the aligner main parts 1g-1l. and the BEKU processing units 8a-8f, 8g-8l. and the development units 7a-7f, and 7g-7l. have been arranged. The above-mentioned example is excellent in maintainability.

[0031] The 3rd example of this invention is explained in drawing 6 . In the 3rd example of this invention, it is the example which separated completely the aligner main parts 1a-1l., and units [the photoresist coating processing units 5a-5l. and the development units 7a-7l.] installation area. The aligner main parts 1a-1f and the aligner main parts 1g-1l. are arranged on both sides of one edge of the interface unit 3, the photoresist coating processing units 5a-5l. and the BEKU processing units 6a-6l. are arranged in one side of the other-end section of the interface unit 3, and it comes to arrange the development units 7a-7l. and the BEKU processing units 8a-8l. in one side of further others.

[0032] The 4th example of this invention is explained in drawing 7 . In the 4th example of this invention, it is the example which dissociated from the aligner main parts 1a-1l., the development units 7a-7l., and the BEKU processing units 8a-8l., and made off-line the photoresist coating processing units 5a-5l. and the BEKU processing units 6a-6l. And as for the photoresist coating processing units 5a-5l. and the BEKU processing units 6a-6l., conveyance is performed by interface unit 3a. Conveyance between the photoresist coating processing units 5a-5l. and the BEKU processing units 6a-6l., the aligner main parts 1a-1l. and the development units 7a-7l., and the BEKU processing units 8a-8l. is performed by the handling unit 9.

[0033] The 5th example of this invention is explained in drawing 8 . In the 5th example of this invention, along with one interface unit 3, the photoresist coating processing units 5a-5l. of photoresist application processing, the BEKU processing units 6a-6l., the aligner main parts 1a-1l. of exposure processing and Racks 2a-2l., the development units 7a-7l. of a development, and the BEKU processing units 8a-8l. are arranged in order of processing, and are constituted. Although it is arranged at one side of the interface unit 3 and the installation distance of equipment becomes long, since equipment is arranged in order of processing, each processing unit is easy to perform maintenance.

[0034] The 6th example of this invention is explained in drawing 9 . In the 5th example of the above, although the development units 7a-7l. and the BEKU processing units 8a-8l. of the photoresist coating processing units 5a-5l., the BEKU processing units 6a-6l., the aligner main parts 1a-1l. of exposure processing, Racks 2a-2l., and a development have been arranged along with one interface unit 3, this example shows the example arranged at the both sides of the interface unit 3. Also in this example, while being arranged in order of processing like the 5th example of the above, the installation distance of equipment can be shortened.

[0035] The 7th example of this invention is explained in drawing 10 . The 7th example is deformation of the 5th example, arranges the aligner main parts 1a-1l. of exposure processing, and Racks 2a-2l. to one side to one interface unit 3, and arranges the photoresist coating processing units 5a-5l., the BEKU processing units 6a-6l., the development units 7a-7l. of a development, and the BEKU processing units 8a-8l. to an another side side.

[0036] The example of the octavus of this invention is explained in drawing 11 . The example of the octavus is an example which used two interface units 3a and 3b. The aligner main parts 1a-1l.

of the photoresist coating processing units 5a-5l., the BEKU processing units 6a-6l., and exposure processing, 1st interface unit 3a connects between Racks 2a-2l. 2nd interface unit 3b connects between the aligner main parts 1a-1l. of exposure processing, Racks 2a-2l., and the development units 7a-7l. of a development and the BEKU processing units 8a-8l. Control of movement of a wafer becomes easy by separating movement of the wafer which faces to the aligner main parts 1a-1l. of exposure processing, and movement of the wafer from the aligner main parts 1a-1l. of exposure processing using the 1st and 2nd interface unit 3b and 3b.

[0037] The 9th example of this invention is explained in drawing 12 . The 9th example as well as the example of the octavus is an example using two interface units 3a and 3b. Two interface units 3a and 3b It is arranged as the aligner main parts 1a-1l. and Racks 2a-2l. are inserted. the photoresist coating processing units 5a-5l. and the BEKU processing units 6a-6l. It is arranged at the 1st interface YUTTO 3a side, and the development units 7a-7l. and the BEKU processing units 8a-8l. are arranged at the 2nd interface unit 3b side.

[0038] The 10th example of this invention is explained in drawing 13 . The 10th example arranges the 9th example annularly. In the center or the periphery section of two interface units 3a and 3b arranged in the shape of a concentric circle, the photoresist coating processing units 5a-5l., The BEKU processing units 6a-6l. or the development units 7a-7l., and the BEKU processing units 8a-8l. are arranged, and the aligner main parts 1a-1l. and Racks 2a-2l. are installed between two interface units 3a and 3b, and it is constituted.

[0039] The 11th example of this invention is explained in drawing 14 . The 11th example connects one unit which comes to arrange the photoresist coating processing units 5a-5l., the BEKU processing units 6a-6l., the aligner main parts 1a-1l., Racks 2a-2l., the development units 7a-7l., and the BEKU processing units 8a-8l. to a radial by the interface unit 3, respectively. It is efficient to usually perform one unit ****** arranged at the radial in this example, and to convey a wafer through the interface unit 3 at the time of abnormalities.

[0040] In addition, this invention is not limited to the above-mentioned example, and based on the meaning of this invention, various deformation is possible for it and it does not eliminate these from the range of this invention.

[0041]

[Effect of the Invention] As mentioned above, according to this invention, the following effects can be done so as explained in detail.

(1) Since relevance can be given between processing units, it becomes possible to set up the number according to the throughput of each processing unit, and generating of the time of the wafer processor limited produced according to the difference of the throughput of a processing unit can be lost.

(2) In the case of a halt of some processing units, a halt of the whole processing line can be prevented by making other processing units distribute processing.

(3) Decline in the efficiency of a phot lithography processes of semiconductor fabrication machines and equipment can be prevented, and productivity can be raised.

[Translation done.]

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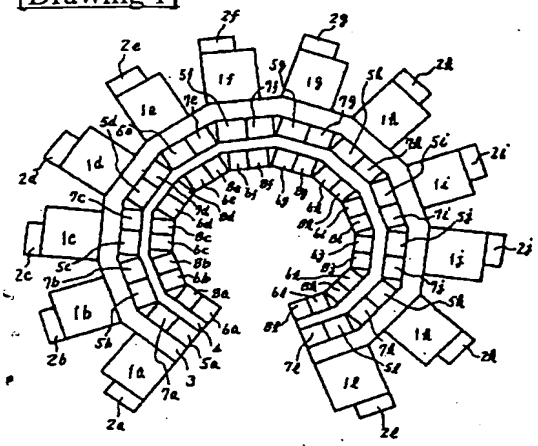
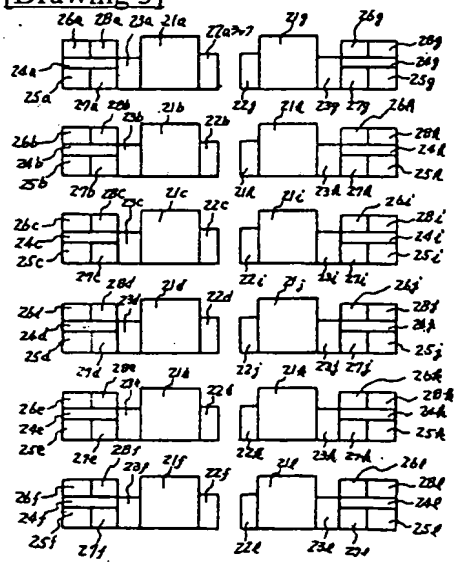
DRAWINGS

[Drawing 1]



1a ～ 1l : 露光装置
2a ～ 2l : ラック
3 : インターフェイスユニット
5a ～ 5l : ホトレジストコーティング処理ユニット
6a ～ 6l : ベーク処理ユニット
7a ～ 7l : 現像処理ユニット
8a ～ 8l : ベーク処理ユニット

[Drawing 3]



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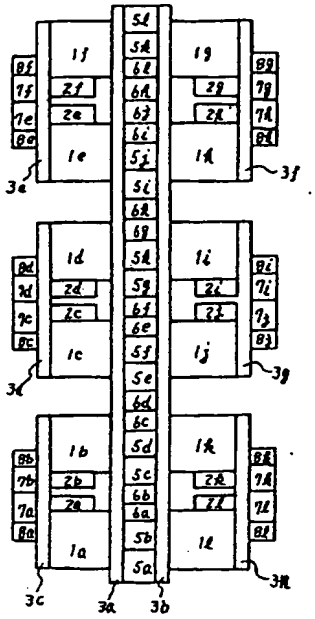
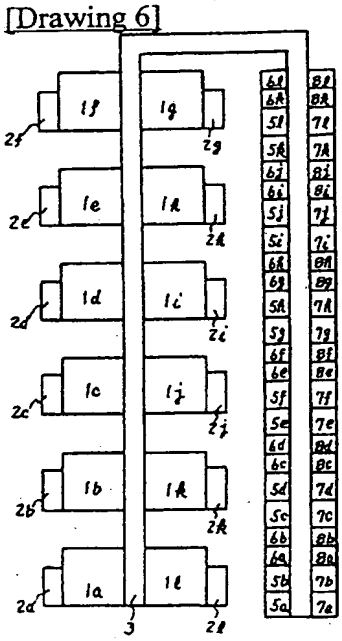
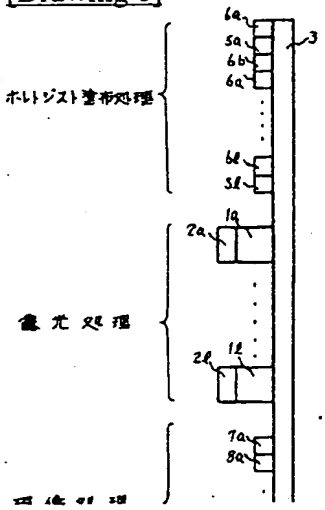
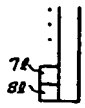


[Drawing 6]



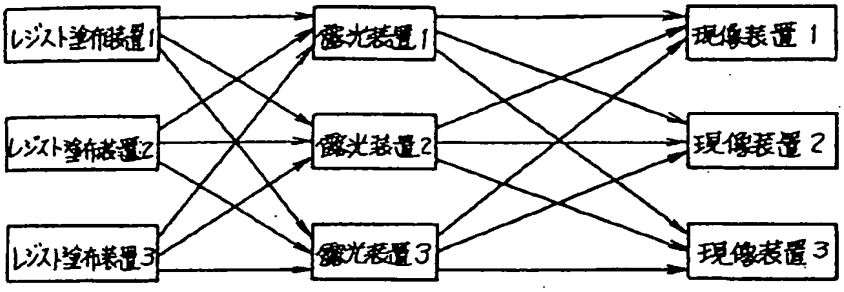
[Drawing 8]



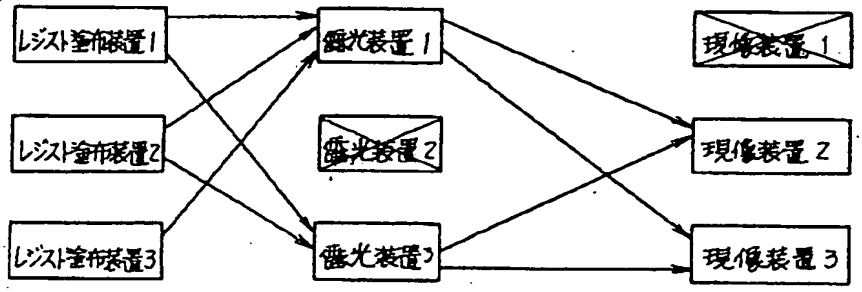


[Drawing 2]

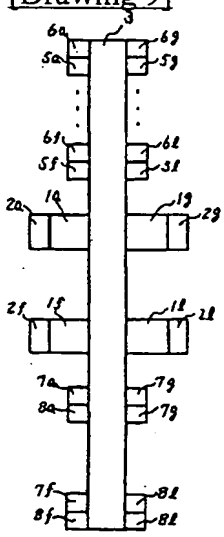
(a)



(b)



[Drawing 9]



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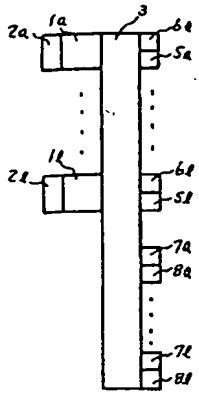

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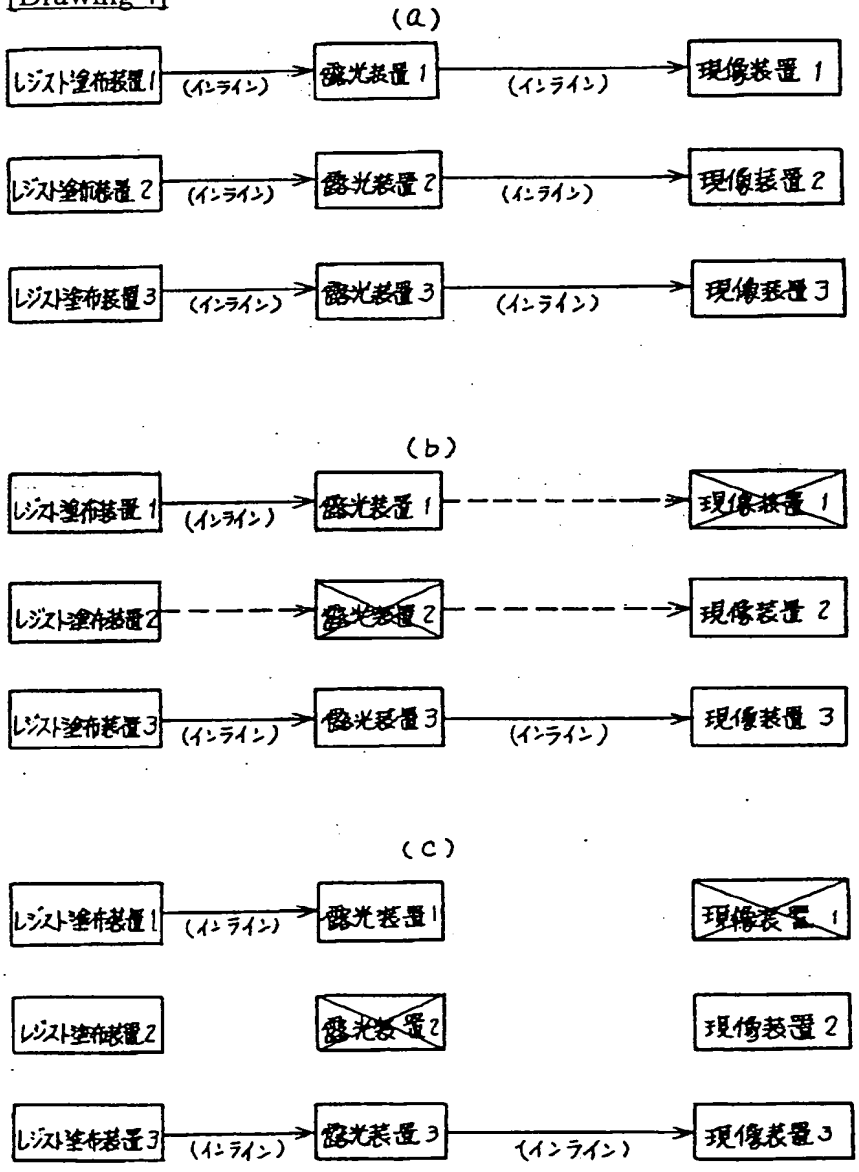

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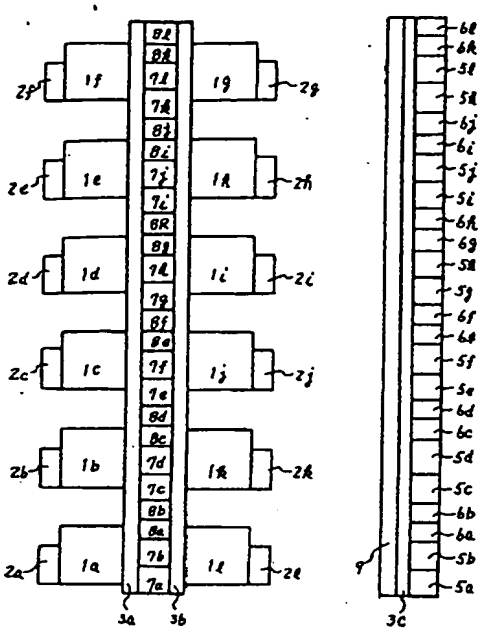
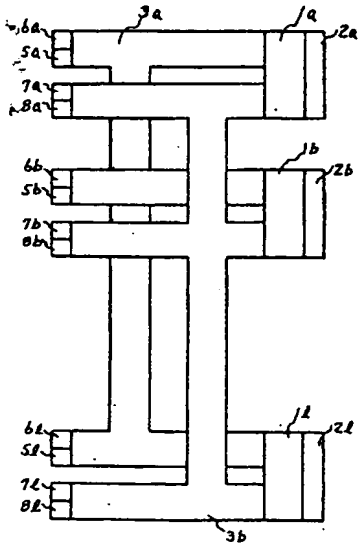


[Drawing 11]



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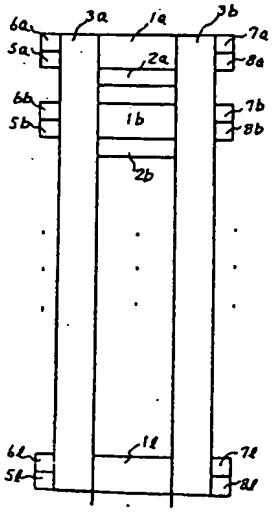

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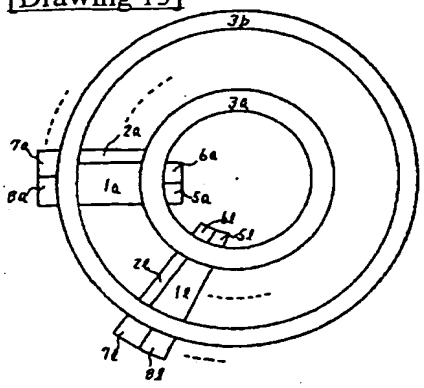

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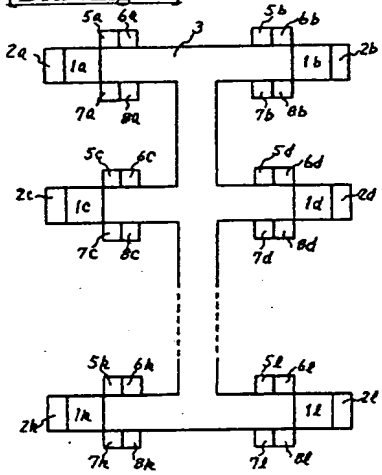

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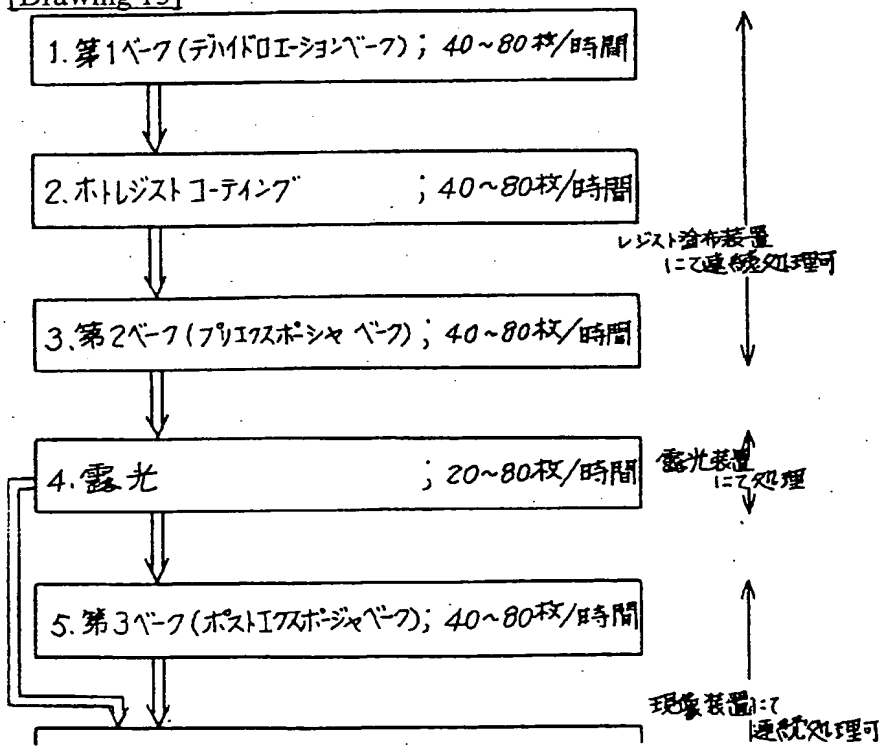

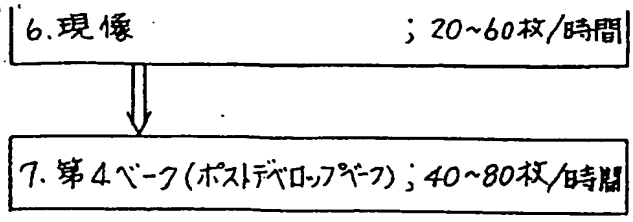

[Translation done.]